CLAIMS

What is claimed is:

1. A data string sample-and-hold method for sampling and holding only series of data which is present during predetermined intervals before and after the arrival time of a predetermined trigger signal, out of a series of data which arrives successively, comprising:

a first step for preparing a primary storage medium in which a first storage area corresponding to the interval before the arrival time of the trigger signal and a second storage area corresponding to the interval after the arrival time of the trigger signal have been defined;

a second step for continuing to write a series of incoming data into the first storage area using wrap-around addressing until the trigger signal arrives; and

a third step for writing a series of data arriving after the arrival of the trigger signal into the second storage area instead of ceasing to write data into the first storage area when the trigger signal arrives.

2. The data string sample-and-hold method according to claim 1, further comprising a fourth step for transferring the data written into the first and second storage areas of the primary storage medium to a secondary storage medium after the completion of the third step.

3. The data string sample-and-hold method according to claim 1, wherein the primary storage medium is a nonvolatile storage medium such as an optical memory suitable for high-speed storage or a volatile storage medium such as a DRAM equipped with back-up power.

4. The data string sample-and-hold method according to claim 2, wherein the primary storage medium is a volatile storage medium such as a DRAM suitable for high-speed storage and secondary storage medium is a nonvolatile storage medium such as a flash memory or hard disk.

5. The data string sample-and-hold method according to any of claims 1 to 4, wherein the storage capacity of the first storage area is an integral multiple of the storage capacity of the second storage area.

6. The data string sample-and-hold method according to claim 5, wherein the storage capacity of the first storage area is twice the storage capacity of the second storage area.

7. A data string sample-and-hold apparatus for sampling and holding only series of data which is present during predetermined intervals before and after the arrival time of a predetermined trigger signal, out of a series of data which arrives successively, comprising:

a primary storage medium;

an area definition data storage means for storing area definition data that defines a first storage area corresponding to the interval before the arrival time of the trigger signal and a second storage area corresponding to the interval after the arrival time of the trigger signal in the primary storage medium;

a first write control means for continuing to write a series of incoming data into the first storage area defined by the area definition data, using wrap-around addressing until the trigger signal arrives; and

a second write control means for writing a series of data arriving after the arrival of the trigger signal into the second storage area defined by the area definition data instead of ceasing to write data into the first storage area when the trigger signal arrives.

8. The data string sample-and-hold apparatus according to claim 7, further comprising:

a secondary storage medium; and

a data transfer control means for transferring the data written into the first and second storage areas of the primary storage medium to the secondary storage medium.

9. The data string sample-and-hold apparatus according to claim 7, wherein the primary storage medium is a nonvolatile storage medium such as an optical memory suitable for

high-speed storage or a volatile storage medium such as a DRAM equipped with back-up power.

10. The data string sample-and-hold apparatus according to claim 8, wherein the primary storage medium is a volatile storage medium such as a DRAM suitable for high-speed storage and secondary storage medium is a nonvolatile storage medium such as a flash memory or hard disk.

11. The data string sample-and-hold apparatus according to any of claims 7 to 10, comprising area definition data generating means for internally generating area definition data based on input data from outside.

12. The data string sample-and-hold apparatus according to claim 11, wherein the input data from outside contains both data indicating the capacity of the first storage area and data indicating the capacity of the second storage area, and the area definition data generating means generates area definition data based on the two sets of data.

13. The data string sample-and-hold apparatus according to claim 11, wherein the input data from outside contains data indicating the capacity of the first storage area, but does not contain data indicating the capacity of the second storage area, and the area definition data generating means generates

area definition data based only on the data indicating the capacity of the first storage area.

14. The data string sample-and-hold apparatus according to any of claims 7 to 13, wherein the storage capacity of the first storage area is an integral multiple of the storage capacity of the second storage area.

15. The data string sample-and-hold apparatus according to claim 14, wherein the storage capacity of the first storage area is twice the storage capacity of the second storage area.

16. A semiconductor integrated circuit comprising:

a first port which is inputted with series of data to be sampled;

a second port which is inputted with predetermined trigger signals;

a third port connected to a predetermined storage medium;

a fourth port which outputs series of sampled and held data;

an area definition data storage means for storing area definition data which defines a first storage area and a second storage area in the storage medium connected to the third port;

a first write control means for continuing to write a series of data inputted through the first port into the first storage area of the storage medium connected to the third port,

using wrap-around addressing until a trigger signal is input through the second port;

a second write control means for writing a series of data arriving after the arrival of the trigger signal into the second storage area of the storage medium instead of ceasing to write data into the first storage area of the storage medium when the trigger signal is inputted through the second port; and

a data read control means for performing control over transmission of data stored in the first storage area and the second storage area of the storage medium connected with the third port to the fourth port.

17. The semiconductor integrated circuit according to claim 16, wherein the storage medium is a nonvolatile storage medium such as an optical memory suitable for high-speed storage or a volatile storage medium such as a DRAM equipped with back-up power.

18. The semiconductor integrated circuit according to claim 16, comprising a power controller for supplying power not only in the semiconductor integrated circuit, but also to the storage medium connected externally, and to an oscillator connected externally and supplies an operation clock to the semiconductor integrated circuit.

19. The semiconductor integrated circuit according to claim 18, comprising an external terminal for connecting a super

capacitor which maintains electric power supplied from the power controller for a predetermined time during a power failure.

20. The semiconductor integrated circuit according to any of claims 16 to 19, further comprising:

a fifth port which is inputted control data; and

an area definition data generating means for internally generating the area definition data based on the control data inputted through the fifth port.

21. A semiconductor integrated circuit comprising:

a first port which is inputted with series of data to be sampled;

a second port which is inputted with predetermined trigger signals;

a third port connected to a predetermined primary storage medium;

a fourth port connected to a predetermined secondary storage medium;

a fifth port which reads sampled and held data;

an area definition data storage means for storing the area definition data which defines a first storage area and a second storage area in the primary storage medium connected to the third port;

a first write control means for continuing to write a series of data inputted through the first port into the first

storage area of the primary storage medium connected to the third port, using wrap-around addressing until a trigger signal is input through the second port;

a second write control means for writing a series of data arriving after the arrival of the trigger signal into the second storage area of the primary storage medium instead of ceasing to write data into the first storage area of the primary storage medium when the trigger signal is inputted through the second port;

a data transfer control means for transferring the data written into the first and second storage areas of the primary storage medium connected with the third port to a secondary storage medium connected with the fourth port; and

a data read control means for performing control over transmission of data stored in the secondary storage medium connected with the fourth port to the fifth port.

22. The semiconductor integrated circuit according to claim 21, wherein the primary storage medium is a volatile storage medium such as a DRAM suitable for high-speed storage and secondary storage medium is a nonvolatile storage medium such as a flash memory or hard disk.

23. The semiconductor integrated circuit according to claim 21, comprising a power controller for supplying power not only in the semiconductor integrated circuit, but also to the primary and secondary storage media connected externally, and

to an oscillator connected externally and supplies an operation clock to the semiconductor integrated circuit.

24. The semiconductor integrated circuit according to claim 23, comprising an external terminal for connecting a super capacitor which maintains electric power supplied from the power controller for a predetermined time during a power failure.

25. The semiconductor integrated circuit according to any of claims 20 to 24, wherein the storage capacity of the first storage area is an integral multiple of the storage capacity of the second storage area.

26. The semiconductor integrated circuit according to claim 25, wherein the storage capacity of the first storage area is twice the storage capacity of the second storage area.

27. The semiconductor integrated circuit according to any of claims 20 to 26, comprising:

a sixth port which is inputted with control data; and

an area definition data generating means for internally generating the area definition data based on the control data input through the sixth port.